Amendments to the Claims:

1-10. (canceled)

11. (currently amended) A method of processing data comprising the steps of:

receiving multiple streams of serial data;

generating from each one of the multiple stream of serial data a group of parallel bit streams;

storing in a computer memory bit patterns representing different groups of parallel bit streams;

searching the memory with a programmed computer to detect a predefined bit pattern stored in each of said different groups;

~~determining~~ measuring misalignment between at least two groups of predefined bit patterns; and

using said programmed computer and the misalignment measurement to adjust the predefined bit patterns between ~~for all~~ selected ones of said groups until said bit patterns are ~~is~~ linearly aligned within said computer memory.

12. (previously presented) The method of claim 11 wherein the predefined bit pattern includes 0101.

13. (currently amended) An apparatus comprising:

N data recovery systems, wherein N > 2 and each one of the data recovery systems being operable to receive a serial data stream from a different communication channel and to generate parallel data streams therefrom; and

an aligner operatively coupled to the N data recovery systems; said aligner being operable to receive the parallel data streams, determine misalignment between groups of bits in different ~~received from each group of the~~ parallel data streams and to adjust the groups of bits between the different parallel data streams relative to one another to remove the misalignment therebetween.

14. (currently amended) The apparatus of claim 13 further including a transmitting subsystem for generating the N serial data streams.

15. (previously presented) The apparatus of claim 14 further including a high speed bus having a plurality of the different communication channel operatively coupling the transmitting sub-system to the N data recovery systems.

16. (currently amended) The apparatus of claim 13 wherein each of the N data recovery systems includes a receiver circuit; and

a nibble recovery circuit operatively coupled to generate one ~~group~~ of the ~~groups of bits~~ parallel data streams.

17. (previously presented) The apparatus of claim 13 wherein the aligner includes M groups of multiple storage devices arranged in parallel; wherein M ≥ 2;

P multiplexers wherein each one of the P multiplexers is operatively coupled to one of the M groups of multiple storage devices; and

a controller that generates control signals that drive each one of the multiplexer to select and output data from one of the coupled multiple storage devices.

18. (currently amended) The apparatus of claim 17 further including a memory operatively coupled to outputs of the P multiplexers and ~~the~~ a controller operatively coupled to the memory.

19. (previously presented) The apparatus of claim 18 wherein each one of the multiple storage devices includes a plurality of serially connected multi-bit latches.

20. (previously presented) A circuit arrangement to align groups of data bits comprising:

M parallel sets of multiple storage devices;

P multiplexers, wherein each of the P multiplexers is operatively connected to a set of the M parallel sets of multiple storage devices;

a memory operatively connected to the P multiplexers, said memory being operable to store the groups of bits outputted from said multiplexers; and

a controller operatively connected to determine the orientation of data in the memory and generate control signals that causes the multiplexers to select storage devices in each of the M parallel sets of multiple storage devices so that data from the selected storage devices are arranged in a predefined orientation within said memory.

21. (previously presented) The circuit arrangement of claim 20 wherein the controller includes a processor executing a program.

22. (previously presented) The circuit arrangement of claim 21 wherein M = 4.

23. (previously presented) The circuit arrangement of claim 20 wherein the predefined orientation is linear.

24. (previously presented) The method of claim 11 wherein bits in each group represents portion of a word.

25. (new) A method of processing data comprising the acts of:

receiving multiple streams of serial data;

generating from each one of the multiple stream of serial data a group of parallel bit streams;

storing in a computer memory the group of parallel bit streams generated for each of one of serial bit stream;

searching the memory with a programmed computer to detect a predefined bit pattern stored in each of said different groups;

measuring misalignment between at least two groups of predefined bit patterns, so found; and

using said programmed computer and the misalignment measurement to adjust the predefined bit pattern between selected ones of said groups until said bit patterns are linearly aligned within said computer memory.